REMARKS

I. Status of Claims

Claims 1-10 remain pending in the application.

In the Office Action, the Examiner objected to the disclosure of the specification.

Claims 1-3 and 6-8 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,440,571 to Mok.

Claims 4, 5, 9 and 10 were also rejected under 35 U.S.C. § 103(a) as being unpatentable over Mok in view of U.S. Patent No. 6,201,789 to Witkowski et al. ("Witkowski").

II. Claim Rejections – 35 U.S.C. § 102(b) and § 103(a)

With respect to independent claims 1 and 6, Mok does not disclose or teach a buffer memory for storing the symbol data for the logical channel according to input sequences so that the symbol data between logical channels are stored in a continuous arrangement; a start address table for storing address information according to the logical channels, each of the address information indicating a location of initial symbol data corresponding to each of the logical channels from among the symbol data stored in the buffer memory; and a multiplexer for selectively outputting the address information stored in the start address table by an enable signal set for each of the logical channels, as claimed.

Mok discloses a buffer memory 200 for receiving digital data transmitted from a host computer, and storing and accessing digital data supplied by a given control signal. There is nothing in Mok that discloses or teaches that the buffer memory 200 stores symbol data for the **logical channel according to input sequences** so that the symbol data between logical channels are stored in a continuous arrangement. For exemplary purposes, the logical

channels of the present application are logical channels of a mobile communication system having different transmission speeds. Accordingly, the digital data transmitted from a computer of Mok is not analogous to symbol data corresponding to logical channels.

Mok also discloses that the buffer memory 200 is filled with a start address capable of starting an encoding operation that is applied to a D flip-flop 1 from a microprocessing unit. The start address is assumed to be 0 and is latched onto a rising edge of a start instruction signal. The D flip-flop 1 generates an output signal which is maintained until a group encoding operation is ended and supplied to an input terminal of a first multiplexer 2. The D flip flop receiving the start address that generates a control signal of Mok is not analogous to a start address table that stores address information according to **the logical channels** in which each of the address information **indicating a location of initial symbol data corresponding to each of the logical channels** from among the symbol data stored in the buffer memory.

Mok further discloses that the multiplexer 2 receives an output signal from the D flip-flop 1. The output signal is maintained until a group encoding operation is ended and supplied to an input terminal of the multiplexer 2. The output signal of the multiplexer 2 is output at a "high" level of a first select signal from a controller. The high level of the first select signal from the controller is not analogous to **an enable signal set for each of the logical channels**. Accordingly, Mok does not disclose or teach claim 1. Likewise, Witkowski does not supply the at least above-noted deficiencies of Mok.

In view of the above arguments, claims 1-3 and 6-8 are not anticipated by Mok, and claims 4, 5, 9 and 10 would not have been obvious from any reasonable combination of Mok and Witkowski. That is, the prior art rejections of claims 1 and 6, as well as dependent claims 2-5 and 7-10, which incorporates all of the limitations of their respective base claims 1 and 6, should be withdrawn based on the above arguments.

CONCLUSION

Applicants submit that the above arguments are fully responsive to the Office Action dated September 17, 2007 and respectfully requests the asserted grounds of rejections be withdrawn based on such arguments.

In view of the above, it is believed that the above-identified application is in condition for allowance, and notice to that effect is respectfully requested. Should the Examiner have any questions, the Examiner is encouraged to contact the undersigned at the telephone number indicated below.

Respectfully submitted,

Demetra Smith-Stewart
Attorney of Record
Reg. No. 47,354

Roylance, Abrams, Berdo & Goodman, L.L.P.
1300 19th Street, N.W., Suite 600
Washington, D.C. 20036-2680
(202) 659-9076

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